CHAPTER 56

TECHNOLOGY
ELECTRONICS & COMMUNICATION
ENGINEERING

Doctoral Theses

01. GUPTA (Akash)
Performance Analysis of Visible Light Communication System Along With Backhaul Solutions and Heterogeneous Networks .
Supervisor : Parul Garg
Th 24770

Abstract
(Verified)

Wound management and wound care has gained importance in recent years. Advances have been made to achieve wound management with better absorption systems using superabsorbent polymers (SAPs). Wound healing is a multi-stage dynamic biological process related to tissue growth and regeneration. SAPs are class of upcoming polymeric material that embraces different biomedical and pharmaceutical applications. Superabsorbent Polymers are three dimensional hydrophilic crosslinked polymeric networks with proficiency to absorb and retain large amount of fluids. SAPs change their volume when in contact with fluids and are termed as Stimuli responsive polymers. Polyaminoacids have been studied in past few years for SAP synthesis. Polyaspartic acid is water soluble and biodegradable polyaminoacid, respond to the change in external environment and are being used as drug delivery system. The work embodied in this thesis focuses on development of superabsorbent polymer synthesized by polyaspartic acid and synthetic monomers. The swelling ability of these polymers are evaluated in physiological fluids and varying pH solutions. The polymer with best absorption ability is exploited further as drug delivery systems (DDS). The peptide GHK-Cu is considered as drug moiety. The healing efficiency of DDS is then evaluated under pre-clinical studies (in vivo). The healing efficacy of the polymer is supported by wound closure, histopathological analysis, biochemical assay.

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02. JANI (Manan)
Performance Analysis of Homogeneous And Heterogeneous Indoor Power Line Communication System .
Supervisor : Prof. Parul Garg
Th 24768

Abstract
(Not Verified)

Power Line Communication (PLC) technology is an emerging technology which allows the transmission of data over the existing powerlines. In recent times, visible light communication (VLC) is a growing communication research field which focuses prominently on using the visible spectrum for the purpose of communication. However, VLC needs to be complemented by a backbone network

for fruitful communication as it is prone to blockages. The ready availability of powerlines make them a good choice for backbone networks for these systems. In the first problem, a PLC system is explored which is corrupted by the combined effects of fading and additive noises. Further, we investigate a multihop cooperative communication over PLC channels using decode and forward (DF) relays between the source and destination nodes. In the next problem, we propose a novel integrated asymmetric relay assisted PLC-VLC system in which the indoor VLC system is connected to a backbone PLC system with the help of a DF relay. The VLC systems are modeled using statistical model employing the uniform distribution for the position of the end users. The third problem deals with the investigation of a novel DF relay assisted cooperative PLC-VLC system where the indoor VLC system employs multiple access points for data transmission. At any particular instant, the user is served with that access point which provides the best instantaneous SNR link for that user. In the fourth problem, we present a novel DF relay assisted PLC-VLC system for Internet of Things (IoT) networks in which the indoor VLC system takes mobility of the end users into account. The VLC channel gain is modeled using random waypoint (RWP) model. The fifth problem deals with the analysis of a spectrally efficient relay assisted PLC-VLC system. Bidirectional communication between the source nodes is achieved with the assistance of two-way relay (TWR).

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03. MISHRA (Shalabh Kumar)

Design And Realization of Fractional Systems For Signal Processing Applications.

Supervisor : Prof. Maneesha Gupta and Prof. Dharmendra Kumar Upadhyay

Th 24771

Abstract
(Not Verfied)

The concept of fractional calculus is one of the most effective mathematical tools for improving the performance of electrical systems; such systems are known as fractional-order systems, and they posesses more degree of freedom, higher accuracy and flexibility than the conventional systems. The fractional-order systems utilize fractance devices (FDs) in place of conventional passive circuit components. These FDs are not available commercially as a lumped element; however they can be approximated using a semi-infinite R-C/R-L tree or ladder network. In this work, an attempt has been made to develop and realize efficient designs of fractional-order circuits and systems for various signal processing applications. Initially, fractional-order low pass filters have been designed and realized using modern current mode active building blocks (ABBs) as an active device. Since, the modern ABBs have higher linearity and dynamic range, more power efficiency, wider bandwidth, and large arithmetic operational capabilities; fractional-order filters realized using these ABBs show improved performance over the existing designs. Further, a compact fractional-order multiphase oscillator has been realized using DVCC (Differential voltage current conveyor) as an active block. This multiphase fractional oscillator provides independent control on the phase and the frequency of the oscillatory waveforms. In addition to this, a novel approach has also been presented to miniaturize the physical structure of fractional-order oscillators by replacing the conventional R-C/R-L tree or ladder network based FDs with an efficient R-C/R-L pair based FDs. The proposed R-C/R-L pair based FDs require only two passive components to approximate an FD. Hence, proposed FDs not only miniaturize the overall circuit but also improve the efficiency, noise performance, and reduce the cost of the fractional-order

system. Finally, a multipurpose electrical system has been designed by cascading logarithmic amplifier with a fractional-order differentiator that can be used in various analog signal (ASP) processing applications

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04. SHWETA KUMARI

Performance Enhancement of Analog Signal Processing Circuits.

Supervisor : Prof. Maneesha Gupta

Th 24769

Abstract
(Verified)

High performance analog signal processing circuit has gained extensive recognition because of increasing demand of portable and high speed devices. In this research work, Voltage Differencing Inverting Buffered Amplifier (VDIBA) and Current Follower Transconductance Amplifier (CFTA) have been selected for performance improvement because they are recent active elements in the field of analog signal processing. The existing VDIBA and CFTA structures operating at low voltage having high transconductance, improved bandwidth and linearity are still not available in literature. In order to enhance the performance of VDIBA circuits, novel methods of transconductance enhancement such as positive feedback techniques along with resistive compensation method for bandwidth extension have been used. Proposed VDIBA I can provide 4.56mS transconductance at bias current (IB) of 300µA. Transconductance of proposed VDIBA II can be enhanced upto 10.6mS at the tuning current (IC) of 100µA. DTMOS transistors have been used for the design of low voltage Fully Balanced VDIBA (FB-VDIBA) which operates at ±0.4V supply voltage. For the design of low voltage high transconductance CFTA circuits, tunable positive feedback and current starving techniques along with Auxiliary Unit (AU) for transconductance enhancement have been used. The proposed CFTA I can provide 8.5mS transconductance at the tuning current (IC) of 110µA. The transconductance of proposed CFTA II is 11.6mS at the tuning current (IC) of 300µA. Low voltage highly linear CFTA III circuit has also been proposed. The linearity of proposed CFTA III has been enhanced by rail to rail input stage and source degeneration technique employed in transconductance stage. Proposed CFTA III provides input dynamic range of ±350µA at the bias current (IB) of 300µA.To illustrate the performance effectiveness of proposed circuits, some new and existing filters and oscillators have been designed and simulated. The TSMC 0.18µm CMOS technology has been used for simulations of all circuits.

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